AMENDMENTS TO THE CLAIMS:

Please amend the claims as follows:

1. – 13. (Cancelled Without Prejudice)

14. (Original) A power spectrum estimator, comprising:

a pulse extraction circuit that compares a digital input signal with a delayed version of the digital input signal to produce an output signal containing extracted pulses;

an averaging circuit receiving the output pulse and producing therefrom an averaged signal representing the averaged value of the output signal;

a subtracter that subtracts a reference signal from the averaged signal to produce a difference signal; and

an absolute value circuit that converts the difference signal to an error signal by taking the absolute value of the difference signal.

15. (Original) The power spectrum estimator according to claim 14, wherein the reference signal comprises a random digital signal passed through a pulse extraction circuit and an averaging circuit.

16. (Original) The power spectrum estimator according to claim 14, wherein the power spectrum estimator estimates the power spectrum using pulse extraction logic circuits that extract pulses of at least one of: one, two and three different pulse widths.

17. (Original) The power spectrum estimator according to claim 14, wherein the averaging circuit comprising a low pass filter.

18. (Original) The power spectrum estimator according to claim 14, further comprising a weighting value multiplier that multiplies a weighting factor by the difference signal before the difference signal is applied to the absolute value circuit.

19. (Original) A power spectrum estimator, comprising:

a pulse extraction circuit that compares a digital input signal with a first delayed version of the digital input signal to produce a first extracted pulse output signal containing extracted pulses of a first pulse width, and compares the digital input signal with a second delayed version of the digital input signal to produce a second extracted pulse output signal containing extracted pulses of a second pulse width;

a first averaging circuit receiving the first extracted pulse output and producing a first averaged value of the output signal to produce a first averaged signal;

a first subtracter that subtracts a first reference signal from the first averaged signal to produce a first difference signal;

a second averaging circuit receiving the second extracted pulse and producing a second averaged value of the output signal to produce a second averaged signal;

a second subtracter that subtracts a second reference signal from the second averaged signal to produce a second difference signal; and

an adder that adds the magnitude of the first difference signal to the magnitude of the second difference signal to produce an output error signal.

20. (Original) A power spectrum estimator according to claim 19, wherein:

the pulse extraction circuit compares the digital input signal with a third delayed version of the digital input signal to produce a third extracted pulse output signal containing extracted pulses of a third pulse width; and further comprising:

a third averaging circuit receiving the third extracted pulse and producing a third averaged value of the output signal to produce a third averaged signal;

a third subtracter that subtracts a third reference signal from the third averaged signal to produce a third difference signal; and

wherein the adder further adds the magnitude of the third error signal to the first and second error signals to produce the output error signal.

21. (Original) The power spectrum estimator according to claim 20, wherein at least one of the first, second and third reference signals comprises a random digital signal passed through a pulse extraction circuit and an averaging circuit.

22. (Original) The power spectrum estimator according to claim 20, wherein the second delayed version of the input signal is delayed by approximately twice the delay of the first delayed version of the input signal, and wherein the third delayed version of the input signal is delayed by approximately three times the delay of the first delayed version of the input signal.

23. (Original) The power spectrum estimator according to claim 20, wherein at least one of the first, second and third averaging circuits comprises a low pass filter.

24. (Original) The power spectrum estimator according to claim 20, further comprising at least one of the following:

a first weighting value multiplier that multiplies a first weighting factor by the first difference signal before the first difference signal is applied to the adder.

a second weighting value multiplier that multiplies a second weighting factor by the second difference signal before the second difference signal is applied to the adder; and

a third weighting value multiplier that multiplies a third weighting factor by the third difference signal before the third difference signal is applied to the adder.

25. (Original) The power spectrum estimator according to claim 19, further comprising a tapped delay line, and wherein the first and second delayed versions of the input signal are produced by passing the input signal through a tapped delay line and extracting the first and second delayed versions of the input signal from delay line taps.

26. (Original) The power spectrum estimator according to claim 25, further comprising one of a phase locked loop and a delay locked loop, that generates a delay correction signal that adjusts the delay of the first and second delayed versions of the input signal.

27. (Original) The power spectrum estimator according to claim 20, wherein the third delayed version of the input signal is produced by passing the input signal through the tapped delay line and extracting the third delayed version of the input signal from a delay line tap.

28. (Original) The power spectrum estimator according to claim 27, further comprising one of a phase locked loop and delay locked loop that generates a delay correction signal that adjusts the delay of the third delayed version of the input signal.

29. (Original) The power spectrum estimator according to claim 19, further comprising:

a finite impulse response filter having tap weight values; and

a tap weight calculator receiving the output error signal and converting the output error signal to adjust the tap weight values.

30. (Currently Amended) An apparatus that estimates power in a signal, comprising:

means for extracting pulses of a specified pulse width from the signal;

means, coupled to the extracting means, for filtering the extracted pulses to produce a filtered pulse signal; ~~and~~

means, coupled to the filtering means, for subtracting the filtered pulse signal from a reference to produce a difference signal as an output, such output representing an estimate of power in the signal; and

generating a coded weight function of the output to control tap weights of a digital filter.

31. (Original) The apparatus according to claim 30, further comprising means, coupled to the subtracting means, for taking the absolute value of the difference signal to represent the estimate of power in the signal.

32. (Original) The apparatus according to claim 30, further comprising means for applying a weighting factor to the difference signal.

33. (Original) The apparatus according to claim 30, further comprising means for converting the estimate of power to a digital value.

34. (Currently Amended) An apparatus that estimates power in a signal, comprising:

means for extracting pulses of a plurality of specified pulse widths from the signal to produce a extracted pulses at each specified pulse width;

means, coupled to the extracting means, for filtering the extracted pulses of each specified pulse width to produce a plurality of filtered pulse signals;

means, coupled to the extracting means, for subtracting each of the filtered pulse signals from a corresponding reference to produce a plurality of difference signals; and

means, coupled to the extracting means, for adding each of the difference signals to produce a sum as an output signal, such output signal representing an estimate of power in the signal, and for generating a coded weight function of the output to control tap weights of a digital filter.

35. (Original) The apparatus according to claim 34, further comprising means for taking the absolute value of each of the difference signals prior to adding.

36. (Original) The apparatus according to claim 34, further comprising means for applying a weighting factor to each of the difference signals prior to the adding.

37. (Original) The apparatus according to claim 34, further comprising means for converting the estimate of power to a digital value.

38. (Original) The apparatus according to claim 34, further comprising means for applying a filter tap weight calculating algorithm to the estimate of power to calculate a filter tap weight value.

39. (Currently Amended) A power spectrum estimator, comprising:

a pulse extraction circuit that compares a digital input signal with a delayed version of the digital input signal to produce an output signal containing extracted pulses;

a counter circuit receiving the output pulse and producing therefrom a count over a time interval representing the averaged value of the output signal;

a subtracter that subtracts a reference count from the averaged signal to produce a difference signal; and

an absolute value circuit that converts the difference signal to an error signal by taking the absolute value of the difference signal.

40. (Original) The power spectrum estimator according to claim 39, wherein the reference signal comprises a random digital signal passed through a counter.

41. (Original) The power spectrum estimator according to claim 39, wherein the power spectrum estimator estimates the power spectrum using pulse extraction logic circuits that extract pulses of at least one of: one, two and three different pulse widths.

42. (Original) The power spectrum estimator according to claim 39, further comprising a weighting value multiplier that multiplies a weighting factor by the difference signal before the difference signal is applied to the absolute value circuit.